ABSTRACT

A controller having programmable delay cells in its input/output channels may also include respective registers storing digital values that control the time delays introduced by the respective delay cells. The values programmed to the registers may be determined by testing the timing of signals between the controller and one or more devices coupled to the channels. The tests may include setting the registers with test values from a set of sequential test values, driving a particular pattern on the signals from the controller to the one or more devices, and checking whether portions of the pattern are received accurately by the one or more devices. Adjusting the timing of the signals may involve centering of the signals with respect to set up and hold time restrictions.